10/16/00

UTILITY PATENT APPLICATION TRANSMITTAL

(Only for new nonprovisional applications under 37 CFR 1.53(b))

Attorney Docket No. **0100.0000780** Total Pages 28
First Inventor or Application Identifier Ho et al.
Title Apparatus for Synchronization of Double Data Rate Signaling
Express Mail Label No. EL504284329US

APPLICATION ELEMENTS *See MPEP chapter 600 concerning utility patent application contents.*	*ADDRESS TO:* **Assistant Commissioner for Patents Box Patent Application Washington, DC 20231**

1. ☒ Fee Transmittal Form
(Submit an original, and a duplicate for fee processing)
2. ☒ Specification *Total Pages* 16
(preferred arrangement set forth below)
- Descriptive title of the Invention
- Cross References to Related Applications
- Statement Regarding Fed sponsored R & D
- Reference to Microfiche Appendix
- Background of the Invention
- Brief Summary of the Invention
- Brief Description of the Drawings *(if filed)*
- Detailed Description
- Claim(s)
- Abstract of the Disclosure

3. ☒ Drawings *(35 USC 113) Total Sheets* 3
4. Oath or Declaration *Total Pages* 3
   a. ☒ Newly executed (original or copy)
   b. ☐ Copy from a prior application (37 CFR 1.63(d))
   (for continuation/divisional with Box 17 completed)
   [Note Box 5 below]
   i. ☐ DELETION OF INVENTOR(S)
   Signed statement attached deleting inventor(s) named in the prior application, see 37 CFR 1.63(d)(2) and 1.33(b).

5. ☐ Microfiche Computer Program *(Appendix)*

6. ☐ Nucleotide and/or Amino Acid Sequence Submission *(if applicable, all necessary)*
   a. ☐ Computer Readable Copy
   b. ☐ Paper Copy (identical to computer copy)
   c. ☐ Statement verifying identity of above copies

ACCOMPANYING APPLICATION PARTS

7. ☒ Assignment Papers (cover sheet & document(s))
8. ☒ 37 CFR 3.73(b) Statement (when there is an assignee) ☒ Power of Attorney
9. ☐ English Translation Document (if applicable)
10. ☐ Information Disclosure Statement (IDS)/PTO-1449 ☐ Copies of IDS Citations
11. ☐ Preliminary Amendment
12. ☒ Return Receipt Postcard (MPEP 503)
(Should be specifically itemized)
13. ☐ Small Entity Statement(s) ☐ Statement filed in Prior Application, Status still proper and desired.
14. ☐ Certified Copy of Priority Document(s)
(if foreign priority is claimed)
15. ☐ Other

16. If a CONTINUING APPLICATION, *check appropriate box and supply the requisite information*
☐ Continuation ☐ Divisional ☐ Continuation-in-part (CIP) of prior application No:
Prior Application Information: Examiner *Group / Art Unit:*

17. CORRESPONDENCE ADDRESS

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Signature		Date	**Oct. 13, 2000**

FEE TRANSMITTAL

Note. Effective October 1, 1997.
Patent fees are subject to annual revision

TOTAL AMOUNT OF PAYMENT ($) 750.00

Complete if Known

Application Number	
Filing Date	**Oct. 13, 2000**
First Named Inventor	**Ho et al.**
Group Art Unit	
Examiner Name	
Attorney Docket Number	**0100.0000780**

METHOD OF PAYMENT (check one)

1. ☒ The Commissioner is hereby authorized to charge indicated fees and credit any over payments to

Deposit Account Number	50-0441
Deposit Account Name	**ATI Technologies, Inc.**

☒ Charge Any Additional Fee Required Under 37 CFR 1.16 and 1.17

☒ Charge the Issue Fee Set in 37 CFR 1.18 at the mailing of the Notice of Allowance

2. ☐ Payment Enclosed:
☐ Check ☐ Money Order ☐ Other

FEE CALCULATION

1. FILING FEE

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
101	690	201	345	Utility filing fee	710.00
106	310	206	155	Design filing fee	
107	480	207	240	Plant filing fee	
108	760	208	380	Reissue filing fee	
114	150	214	75	Provisional filing fee	

SUBTOTAL (1) ($) 710.00

2. CLAIMS

Claims	Extra	Fee from below	Fee Paid
Total **18**	(-20 =)		
Indep. **3**	(- 3 =)		
Multiple Dep			

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description
103	18	203	9	Claims in excess of 20
102	78	202	39	Independent claims in excess of 3
104	260	204	130	Multiple dependent claim
109	78	209	39	Reissue independent claims over original patent
110	18	210	9	Reissue claims in excess of 20 and over original patent

SUBTOTAL (2) ($) _____

FEE CALCULATION (continued)

3. ADDITIONAL FEES

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
105	130	205	65	Surcharge - late filing fee or oath	
127	50	227	25	Surcharge - late provisional filing fee or cover sheet	
139	130	139	130	Non-English specification	
147	2,520	147	2,520	For filing a request for reexamination	
112	920*	112	920*	Requesting publication of SIR prior to Examiner action	
113	1,840*	113	1,840*	Requesting publication of SIR after Examiner action	
115	110	215	55	Extension for reply within first month	
116	380	216	190	Extension for reply within second month	
117	870	217	435	Extension for reply within third month	
118	1,360	218	680	Extension for reply within fourth month	
128	1,850	228	925	Extension for reply within fifth month	
119	300	219	150	Notice of Appeal	
120	300	220	150	Filing a brief in support of an appeal	
121	260	221	130	Request for oral hearing	
138	1,510	138	1,510	Petition to institute a public use proceeding	
140	110	240	55	Petition to revive - unavoidable	
141	1,210	241	605	Petition to revive - unintentional	
142	1,210	242	605	Utility issue fee (or reissue)	
143	430	243	215	Design issue fee	
144	580	244	290	Plant issue fee	
122	130	122	130	Petitions to the Commissioner	
123	50	123	50	Petitions related to provisional applications	
126	240	126	240	Submission of Information Disclosure Stmt	
581	40	581	40	Recording each patent assignment per property (times number of properties)	40.00
146	690	246	345	Filing a submission after final rejection (37 CFR 1.129(a))	
149	690	249	345	For each additional invention to be examined (37 CFR 1.129(b))	
Other fee (specify)					
Other fee (specify)					

*Reduced by Basic Filing Fee Paid

SUBTOTAL (3) ($) 40.00

SUBMITTED BY: MARKISON & RECKAMP, P.C.				Complete (if applicable)	
Typed or Printed Name	**Christopher J. Reckamp**			Reg. Number	**34,414**
Signature		Date	**10/13/00**	Deposit Account User ID	**50-0441**

PATENT APPLICATION
DOCKET NO. 0100.000078

In the United States Patent and Trademark Office

FILING OF A UNITED STATES PATENT APPLICATION

Title:

APPARATUS FOR SYNCHRONIZATION OF DOUBLE DATA RATE SIGNALING

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EL 504284329 US

Date of Deposit: 10/13/00

I hereby certify that this paper is being deposited with the U.S. Postal Service "Express Mail Post Office to Addresses" service under 37 C.F.R. Section 1.10 on the 'Date of Deposit', indicated above, and is addressed to the Commissioner of Patents and Trademarks, Washington, D C. 20231.

Name of Depositor Rosalie Swanson
(print or type)

Signature Rosalie Swanson

APPARATUS FOR SYNCHRONIZATION OF DOUBLE DATA RATE SIGNALING

Field Of The Invention

The invention relates generally to synchronization circuits and methods and more particularly to synchronization circuits and methods used with double data rate transfer schemes.

Background Of The Invention

Memory chips are known that employ a double data rate (DDR) communication scheme. Such a memory may be used in any suitable apparatus including, for example, a graphics acceleration system employing one or more graphics chips that sending information to and retrieve data from a memory, such as a frame buffer. Memory interface circuits for facilitating a double data rate communication scheme are also known.

With double data rate communication schemes, a DATA signal, STROBE signal and CLOCK signal are used to communicate data to and from a memory such as between a memory and another circuit such as a graphics accelerator, CPU or any other suitable circuit. With double data rate schemes, typically, the memory chip, such as a DDR SDRAM (double data rate synchronous DRAM) typically expects a DATA signal to be sent to the memory chip, from a graphics chip for example, together with a special STROBE signal. Typically, the STROBE signal has the same frequency as the CLOCK signal that is generated by, for example, the graphics chip, or other suitable circuit. The DATA signal is synchronized with the CLOCK signal. The STROBE signal is typically sent so that the strobe pulse occurs in the middle of a DATA signal window. This occurs typically when the graphics chip is sending data to the memory. Accordingly, the

STROBE signal is typically sent later by a quarter of the clock period compared to the DATA signal. This offset allows input memory flip flops to receive the data.

In receiving mode, when the graphics chip or other circuit is receiving data from memory, the memory chip generates and sends the STROBE and DATA signals back. However, typical double data rate interface requirements require the memory chip to send the STROBE and DATA signals simultaneously to simplify the on board memory chip circuitry. Accordingly, a receiving circuit, such as a graphics chip or other suitable circuit, has to delay internally, the received STROBE signal that was sent from the memory chip to provide the same conditions for the receiving circuit input flip flop as for the sending circuits. In other words, the received STROBE signal that is actually is the clock input of the graphics chip flip flop has to be in the middle of the data signal window. This time offset has to be stable, including over temperature changes, voltage changes and fabrication process variations.

One approach to providing a requisite delay in the receiving circuit includes a delay circuit that uses several inverters to delay the STROBE signal. The time delay can be adjusted to be a quarter of the clock period (according to typical DDR interface requirements, the data signal has to be received at the rising and falling edge of the STROBE signal). However, in the case where the time delay is temperature, voltage or process dependent, a variable delay in the offset STROBE signal can occur. This can result in loss of data.

For example, FIG. 1 is a diagrammatic illustration of one example of a signal phase shifting circuit 10 that suitably phase shifts a received input signal 12, such as a received STROBE signal, back, for example, a quarter of a CLOCK period so that received data 14 is suitably latched by a latch circuit 16 before the data is passed to core logic 18. A reference signal 20, such as the CLOCK signal, is received by a reference signal period dividing circuit 22. The reference signal period dividing circuit 22 provides a delay control signal 26 that is a voltage controlled delay control signal, to a variable delay circuit 28.

The reference signal period dividing circuit 22 is configured as a type of DLL (delay lock loop). The DLL consists of a phase frequency detector 30, a low pass filter 32, a charge pump 34 and a voltage controlled delay line 37 having several serially connected voltage controlled buffers 36a-36n. With this configuration the propagation time delay between the input of the voltage control delay line 37 and the output of the voltage control delay line 37 is equal to the clock period. The DLL 22 operates, as known in the art, with internal negative feedback. If the reference clock period is not changing, then the DLL will provide synchronization within a reasonable temperature, voltage and fabrication process variation. The phase detector 30 will change the delay control voltage 26 of the voltage control delay line 37 to provide a change any time the clock period time delay between the input of the VCDL 37 and its output is more than one clock period. The delay control voltage will be different with different temperatures, supply voltages or fabrication process variation.

The input signal 12, in this example the STROBE signal, is received by receiver buffer 38 and passed to the variable delay circuit 28 which also employs another voltage control delay line 40 that is commonly controlled by the same delay control signal 26. Since printed circuit board layouts and on chip layouts can add additional delays, the multiplexer 42 and phase shifted output signal drive buffer 44 are used as a delay stage to vary a delay setting of the variable delay circuit 28 to allow selection of delay to compensate for additional printed circuit board layout delays, if desired. A control register 46 is used to control select lines 48 to select the amount of delay required to provide a quarter clock delay or phase shift between the input signal 12 and the shifted signal 50. This allows a type of step control to accurately obtain the requisite STROBE signal in the receiving circuit once the circuit board has been laid out.

As shown, the signal phase shifting circuit 10 can be considered to have a delay lock loop with two voltage control delay lines 40 and 37. Both of them are controlled by the same delay control voltage 26 and they are made of the same delay elements except the voltage control delay line 37 has four times the number of delay elements as the delay

line 40. The shorter delay line is used to delay the STROBE signal by a quarter of the memory clock period. Accordingly, since the STROBE signal has the same frequency as the memory clock, and since each STROBE signal represents one valid data cycle, the "quarter delay" will place the STROBE signal in the middle of the data window.

A problem arises since the multiplexer 42 and buffer 44 can shift over temperature and at high frequencies, thereby destabilizing the signal phase shifting required for the STROBE signal.

Another approach may be to have a separate strobe line for every data pad to duplicate the delay chain for every data line. However, a problem can arise due to the phase shift in the STROBE signal and would drastically increase the complexity in fabrication costs of the device. It is desirable to have a constant offset regardless of the supply voltage variations, temperature variations and fabrication process variations.

Accordingly, a need exists for an improved apparatus to facilitate double data rate signaling.

Brief Description Of The Drawings

The invention will be more readily understood with reference to the following drawings wherein:

FIG. 1 is a block diagram illustrating a known signal phase shifting circuit used in a double data rate receiving interface circuit;

FIG. 2 is a block diagram illustrating one example of a signal phase shifting circuit in accordance with one embodiment of the invention; and

FIG. 3 is a block diagram illustrating one example of a signal phase shifting circuit in accordance with one embodiment of the invention.

Detailed Description Of a Preferred Embodiment of The Invention

A signal phase shifting circuit is shifts the phase of an input signal, such as a STROBE signal, based on a reference signal, such as a CLOCK signal, to facilitate, for

example, receiving of double data rate data. The signal phase shifting circuit includes a reference signal period dividing circuit having a feedback delay matching array operatively coupled to one of a plurality of voltage control delay lines (VCDL). The signal phase shifting circuit also includes a variable delay circuit that provides a phase shifted output signal, such as a phase shifted STROBE signal, that includes a delay stage and a phase shifted output signal drive buffer coupled to the delay stage, such as a voltage control delay line. The feedback delay matching array includes a plurality of serially coupled buffer stages operatively coupled to compensate for delay variations associated with the phase shifted output signal drive buffer in the variable delay circuit. Accordingly, a more stable STROBE signal phase shift occurs that is less sensitive to temperature and voltage variations while still allowing the compensation of delay due to, for example, printed circuit board layout delays and other delays.

FIG. 2 illustrates a signal phase shifting circuit 200 that includes a reference signal period dividing circuit 202 that includes the phase shift generating circuit 22 and a feedback delay matching array 204 that is operatively coupled to an output 206 of the phase shift generating circuit 22. The feedback delay matching array 204 receives a phase shifted reference signal 208 produced by the phase shift generating circuit 22. The feedback delay matching array 204 produces a feedback control signal 210 that is fed back to the phase shift generating circuit 22. The feedback control signal 210 is delayed by the delay matching array 204.

The reference signal period dividing circuit 202 includes a first input 212 that receives the reference signal 20, such as a CLOCK signal, a second input 214 that receives the feedback control signal 210. The phase shift generating circuit 22 is operatively responsive to the reference signal 20 and to the feedback control signal 210 to phase shift the reference signal 20 to produce the phase shifted reference signal 208.

The signal phase shifting circuit 200 also includes the variable delay circuit 40 that includes an input 220 that receives the input signal 12, such as the STROBE signal. The variable delay circuit 40 is also operatively responsive to the delay control signal 222

produced by the phase shift generating circuit 22 to vary the delay provided by the variable delay circuit 40.

The feedback delay matching array 204 compensates for delay variations associated with the phase shifted output signal drive buffer 44 and multiplexer 42. In addition, the feedback delay matching array 204 matches the delay associated with the signal drive buffer 44 and the multiplexer 42.

The reference signal period dividing circuit 202 also includes an output 226 that provides the delay control signal 222 for the variable delay circuit 40. The variable delay circuit 40 provides the phase shifted output signal 50 (STROBE signal) through the multiplexer 42 and buffer 44.

Referring to FIG. 3, in one embodiment, the feedback delay matching array 204 includes a plurality of serially coupled buffer stages 302a, 302b, 302c and 302d that are operatively coupled to compensate for delay variations associated with the phase shifted output signal buffer 44 and the multiplexer 42. In this example, there are four buffer stages as well as four multiplexer stages. Also in this embodiment the feedback delay matching array 204 includes a plurality of serially coupled multiplexers 304a-304d. The multiplexer and buffer stages 302 and 304 are operatively coupled to compensate for delay variations associated with the multiplexer 42 and the phase shifted output signal drive buffer 44 in the variable delay circuit. This circuit shifts a received STROBE signal by a quarter of the CLOCK period. Voltage controlled delay 37 together with the feedback delay matching array 204 have a total delay that equals the CLOCK period. By using only a quarter of the voltage controlled buffers 36a-36n, as well as a quarter of the serially coupled buffer stages 302a-302d, and a quarter of serially coupled multiplexers 304a-304d, the STROBE signal can be shifted by precisely a quarter of the CLOCK period. Ifa half of the CLOCK period shift is needed for the STROBE signal, the circuit should provide serial connection with the voltage controlled delay using only two multiplexers and two buffer stages, and after that only a half of them are used to shift the STROBE signal.

As shown, the multiplexer 42 and drive buffer 44 are shown functionally since a plurality may be used, if desired. It will be recognized that any suitable number of multiplexer and buffer stages may be used depending upon for example PCB layout delays. The multiplexers 304a-304d are suitably enabled through enable lines 306 under control of a suitable control register and any other suitable mechanism.

The variable delay circuit 28 also includes the multiplexer 42 and output signal drive buffer 44, as well as the delay stage buffers 41a-41n. The multiplexer 42 is operatively coupled to vary the delay setting of a variable delay stage 40 by selectively switching between different numbers of delay buffers 41a-41n. This is done by controlling the select lines 48 through control register 46 or through any other suitable mechanism.

The latch circuit 16 serves as a data latch having an input 320 that is operatively coupled to receive the data 14, and a second input 322 operatively coupled to receive the phase shifted output signal 50 so received data is appropriately latched with respect to the phase adjusted STROBE signal. As noted above, the STROBE signal is associated with a double data rate communication. For example, it may be generated by a double data rate memory device.

The phase shift generating circuit 22 that includes the serially coupled buffers 36a-36n has output 208 of the control delay stage passed to the feedback delay matching array 204 which attempts to match the delay presented by circuits 42 and 44.

The phase shift generating circuit 22 includes the phase frequency detector circuit 30 that compares the reference signal 20 with the feedback control signal 210. The charge pump 34 is operatively coupled to the phase frequency detector 30 to receive an up count 330 or down count 332 for the charge pump circuit 34 depending upon the amount of difference in phases. The loop filter (low pass filter 32) receives the output

334 from the charge pump circuit 34 and provides delay control signal 26 for the variable delay circuit 40 and for the circuit 37.

The above-described phase shifting circuit provides a feedback delay matching array that is operatively coupled to one of a plurality of voltage control delay lines to compensate for delay variations associated with phase shifted output signal driver and/or any associated multiplexers or circuits associated with the phase shifted output signal driver buffer. Accordingly, a more stable STROBE phase shifting circuit is provided for a receiver used for double data rate communications.

It should be understood that the implementation of other variations and modifications of the invention in its various aspects will be apparent to those of ordinary skill in the art, and that the invention is not limited by the specific embodiments described. It is therefore contemplated to cover by the present invention, any and all modifications, variations, or equivalents that fall within the spirit and scope of the basic underlying principles disclosed and claimed herein.

Claims

WHAT IS CLAIMED IS:

1. A signal phase shifting circuit operative to shift the phase of an input signal based on a reference signal comprising:

a reference signal period dividing circuit having:

a first input that receives the reference signal,

a second input that receives a feedback control signal,

a phase shift generating circuit operatively responsive to the reference signal and the feedback control signal;

an output that provides a voltage controlled delay control signal for a variable delay circuit, and

a feedback delay matching array operatively coupled to an output of the phase shift generating circuit, that produces the feedback control signal; and

the variable delay circuit including an input that receives the input signal and being operatively responsive to the delay control signal, to provide a phase shifted output signal of the input signal.

2. The signal phase shifting circuit of claim 1 wherein the variable delay circuit includes a delay stage and at least one phase shifted output signal drive buffer operatively coupled to the delay stage.

3. The signal phase shifting circuit of claim 2 wherein the feedback delay matching array includes a plurality of serially coupled buffer stages operatively coupled to compensate for delay variations associated with the at least one phase shifted output signal drive buffer.

4. The signal phase shifting circuit of claim 1 wherein the variable delay circuit includes a delay stage and at least one mulitplexer operatively coupled to vary a

delay setting of the variable delay stage, and at least one phase shifted output signal drive buffer operatively coupled to an output of the at least one mulitplexer.

5. The signal phase shifting circuit of claim 4 wherein the feedback delay matching array includes a plurality of serially coupled mulitplexer and buffer stages operatively coupled to compensate for delay variations associated with the at least one mulitplexer and the at least one phase shifted output signal drive buffer in the variable delay circuit.

6. The signal phase shifting circuit of claim 1 including a data latch having a first input operatively coupled to receive data, and a second input operatively coupled to receive the phase shifted output signal.

7. The signal phase shifting circuit of claim 1 wherein the reference signal is a CLOCK signal and wherein the input signal is a STROBE signal and wherein the phase shifted output signal is a phase shifted STROBE signal associated with a double data rate communication.

8. The signal phase shifting circuit of claim 1 wherein the phase shift generating circuit includes a plurality of serially coupled buffers that form a controlled delay stage and wherein the feedback delay matching array includes a plurality of serially coupled mulitplexer and buffer stages operatively coupled to the plurality of serially coupled buffers.

9. A signal phase shifting circuit operative to shift the phase of a strobe signal based on a reference signal comprising:

a reference signal period dividing circuit having:

a first input that receives the reference signal,

a second input that receives a feedback control signal,

a phase shift generating circuit that includes a delay lock loop circuit operatively responsive to the reference signal and the feedback control signal wherein the delay lock loop circuit includes:

a phase/frequency detection circuit that compares the reference signal and the feedback control signal,

a charge pump circuit operatively coupled to the phase/frequency detection circuit, and

a loop filter operatively responsive to an output from the charge pump circuit, that provides a delay control signal for a variable delay circuit, and

a feedback delay matching array operatively coupled to an output of the phase shift generating circuit, that produces the feedback control signal; and

the variable delay circuit including an input that receives the input signal and being operatively responsive to the delay control signal, to provide a phase shifted output signal.

10. The signal phase shifting circuit of claim 9 wherein the variable delay circuit includes a delay stage and at least one mulitplexer operatively coupled to vary a delay setting of the variable delay stage, and at least one phase shifted output signal drive buffer operatively coupled to an output of the at least one mulitplexer.

11. The signal phase shifting circuit of claim 10 wherein the feedback delay matching array includes a plurality of serially coupled mulitplexer and buffer stages operatively coupled to compensate for delay variations associated with the at least

one mulitplexer and the at least one phase shifted output signal drive buffer in the variable delay circuit.

12. The signal phase shifting circuit of claim 9 wherein the reference signal is a CLOCK signal and wherein the input signal is a STROBE signal and wherein the phase shifted output signal is a phase shifted STROBE signal associated with a double data rate communication.

13. The signal phase shifting circuit of claim 9 wherein the phase shift generating circuit includes a plurality of serially coupled buffers that form a controlled delay stage and wherein the feedback delay matching array includes a plurality of serially coupled mulitplexer and buffer stages operatively coupled to the plurality of serially coupled buffers.

14. A data receiving circuit having a signal phase shifting circuit operative to shift the phase of a strobe signal based on a reference signal comprising:

a reference signal period dividing circuit having:

a first input that receives the reference signal,

a second input that receives a feedback control signal,

a phase shift generating circuit that includes a delay lock loop circuit operatively responsive to the reference signal and the feedback control signal wherein the delay lock loop circuit includes:

a phase/frequency detection circuit that compares the reference signal and the feedback control signal,

a charge pump circuit operatively coupled to the phase/frequency detection circuit, and

a loop filter operatively responsive to an output from the charge pump circuit, that provides a control signal for a variable delay circuit, and

a feedback delay matching array operatively coupled to an output of the phase shift generating circuit, that produces the feedback control signal;

the variable delay circuit being operatively responsive to the control signal that provides a phase shifted output signal, and including an input that receives the input signal; and

a data latch having a first input operatively coupled to receive data, and a second input operatively coupled to receive the phase shifted output signal.

15. The signal phase shifting circuit of claim 14 wherein the variable delay circuit includes a delay stage and at least one mulitplexer operatively coupled to vary a delay setting of the variable delay stage, and at least one phase shifted output signal drive buffer operatively coupled to an output of the at least one mulitplexer.

16. The signal phase shifting circuit of claim 15 wherein the feedback delay matching array includes a plurality of serially coupled mulitplexer and buffer stages

operatively coupled to compensate for delay variations associated with the at least one mulitplexer and the at least one phase shifted output signal drive buffer in the variable delay circuit.

17. The signal phase shifting circuit of claim 15 wherein the reference signal is a CLOCK signal and wherein the input signal is a STROBE signal and wherein the phase shifted output signal is a phase shifted STROBE signal associated with a double data rate communication.

18. The signal phase shifting circuit of claim 14 wherein the phase shift generating circuit includes a plurality of serially coupled buffers that form a controlled delay stage and wherein the feedback delay matching array includes a plurality of serially coupled mulitplexer and buffer stages operatively coupled to the plurality of serially coupled buffers.

APPARATUS FOR SYNCHRONIZATION OF DOUBLE DATA RATE SIGNALING

Abstract Of The Disclosure

A signal phase shifting circuit shifts the phase of an input signal, such as a STROBE signal, based on a reference signal, such as a CLOCK signal, to facilitate, for example, receiving of double data rate data. The signal phase shifting circuit includes a reference signal period dividing circuit having a feedback delay matching array operatively coupled to one of a plurality of voltage control delay lines. This signal phase shifting circuit also includes a variable delay circuit that provides a phase shifted output signal, such as a phase shifted STROBE signal, that includes a delay stage in a phase shifted output signal drive buffer coupled to the delay stage, such as a voltage control delay line. The feedback delay matching array includes a plurality of serially coupled buffer stages operatively coupled to compensate for delay variations associated with the phase shifted output signal drive buffer in the variable delay circuit. Accordingly, a more stable STROBE signal phase shift occurs that is less sensitive to temperature and voltage variations while still allowing the compensation of delay due to, for example, printed circuit board layout delays and other delays.

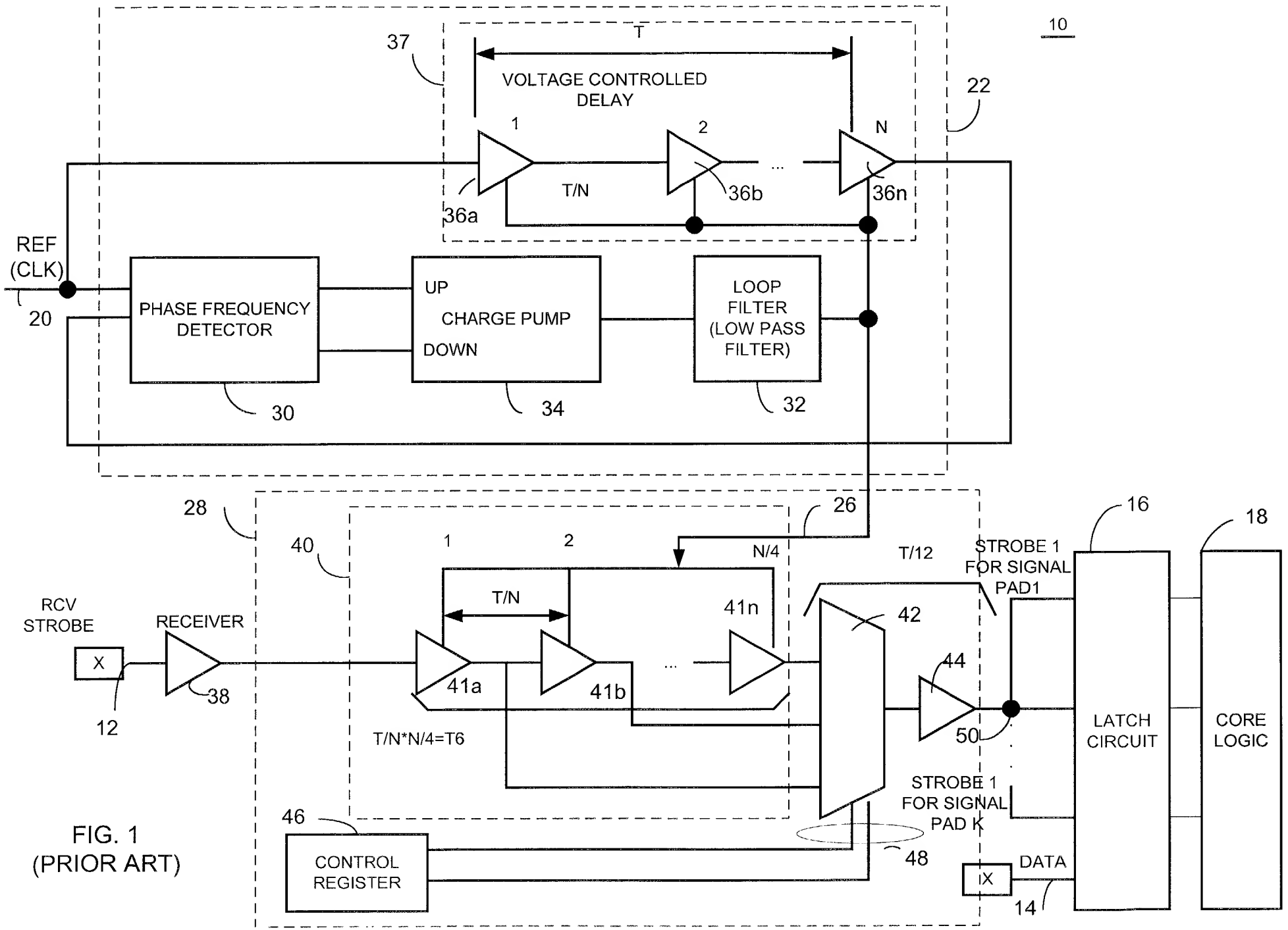

FIG. 1
(PRIOR ART)

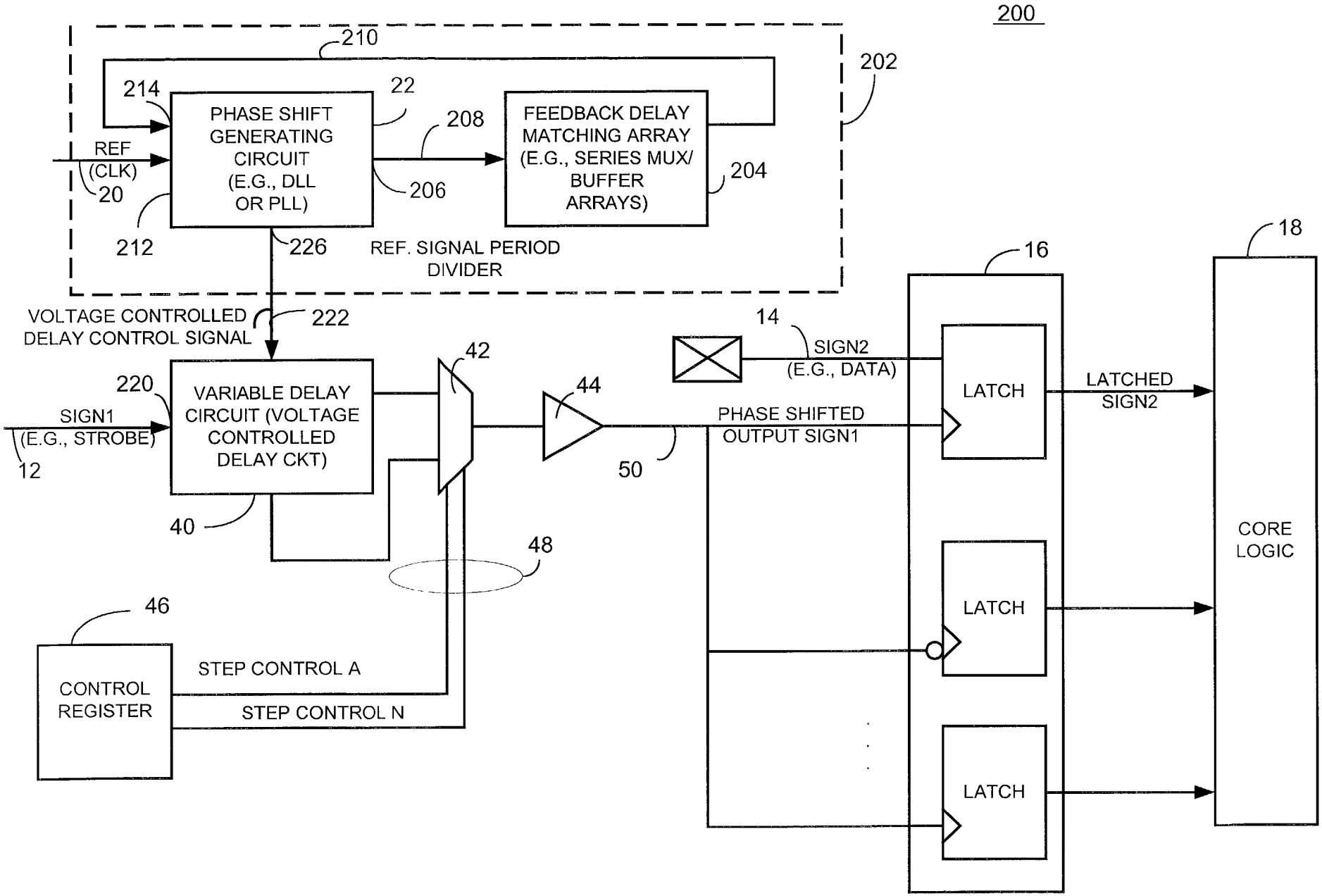
200
210
202
214
22
208
PHASE SHIFT GENERATING CIRCUIT (E.G., DLL OR PLL)
FEEDBACK DELAY MATCHING ARRAY (E.G., SERIES MUX/ BUFFER ARRAYS)
204
REF (CLK)
20
206
212
226
REF. SIGNAL PERIOD DIVIDER
VOLTAGE CONTROLLED DELAY CONTROL SIGNAL
222
16
18
14
SIGN2 (E.G., DATA)
42
220
VARIABLE DELAY CIRCUIT (VOLTAGE CONTROLLED DELAY CKT)
44
LATCH
LATCHED SIGN2
SIGN1 (E.G., STROBE)
12
PHASE SHIFTED OUTPUT SIGN1
50
40
48
CORE LOGIC
LATCH
46
CONTROL REGISTER
STEP CONTROL A
STEP CONTROL N
LATCH

FIG. 2

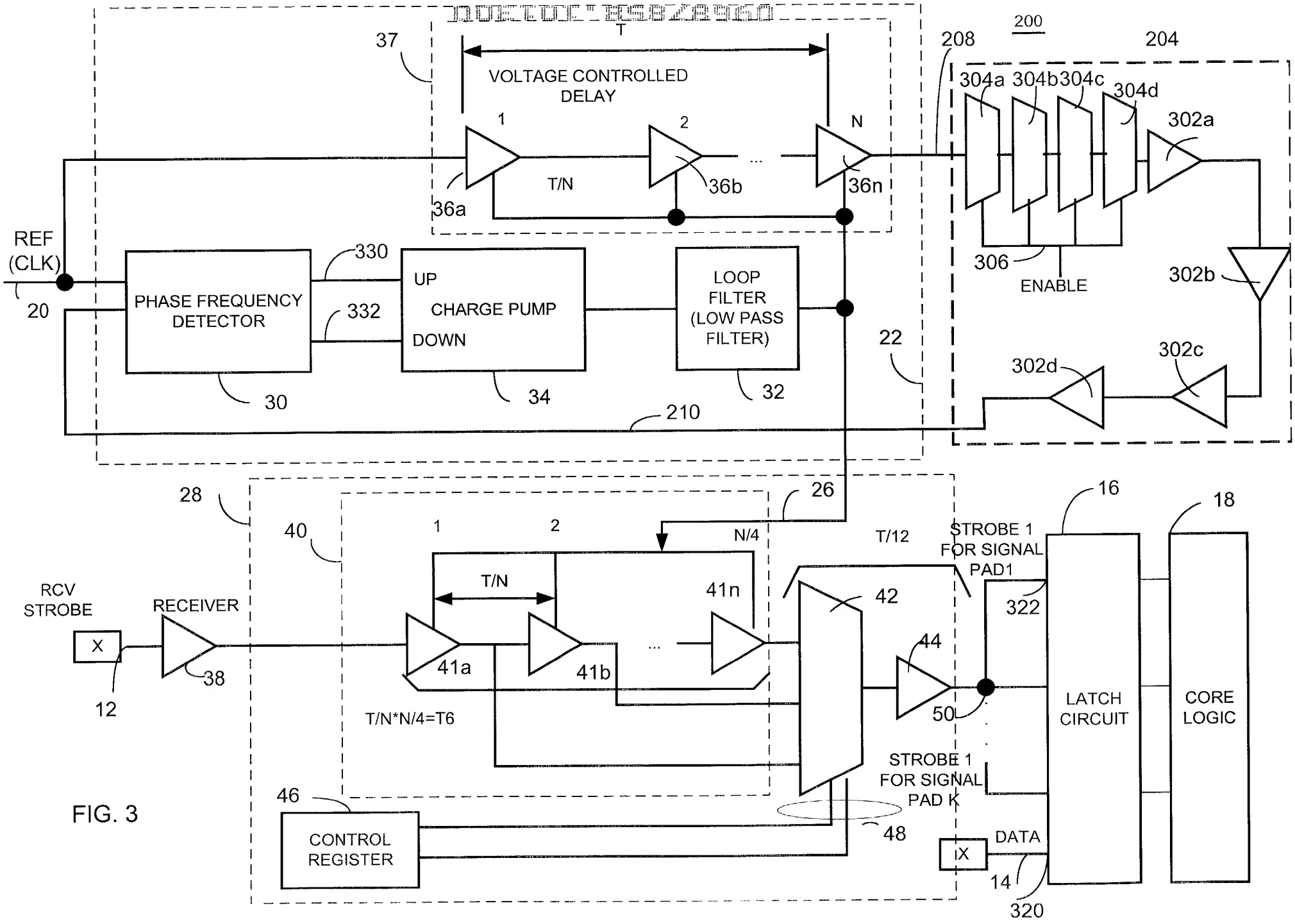
200
37
T
VOLTAGE CONTROLLED DELAY
1
2
N
T/N
36a
36b
36n
208
204
304a
304b
304c
304d
302a
302b
302c
302d
306
ENABLE
REF (CLK)
20
PHASE FREQUENCY DETECTOR
330
332
UP
CHARGE PUMP
DOWN
LOOP FILTER (LOW PASS FILTER)
30
34
32
22
210
28
40
26
1
2
N/4
T/12
T/N
41n
41a
41b
T/N*N/4=T6
RCV STROBE
RECEIVER
X
12
38
42
44
50
STROBE 1 FOR SIGNAL PAD1
322
16
18
LATCH CIRCUIT
CORE LOGIC
STROBE 1 FOR SIGNAL PAD K
46
CONTROL REGISTER
48
X
DATA
14
320

FIG. 3

DECLARATION FOR UTILITY OR DESIGN PATENT APPLICATION

(37 CFR 1.63)

☒ Declaration Submitted with Initial Filing, OR
☐ Declaration Submitted after Initial Filing
(surcharge (37 CFR 1.16 (e)) required)

Attorney Docket Number 0100.0000780
First Named Inventor Chak Cheung Edward Ho
COMPLETE IF KNOWN
Application Number
Filing Date
Group Art Unit
Examiner Name

As a below named inventor, I hereby declare that:
My residence, post office address, and citizenship are as stated below next to my name.
I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled:
APPARATUS FOR SYNCHORNIZATION OF DOUBLE DATA RATE SIGNALING
the specification of which:
☒ is attached hereto.
☐ was file on (MM/DD/YYYY) as United States Application Number or PCT International Application Number and was amended on (MM/DD/YYYY) (if applicable).

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment specifically referred to above.
I acknowledge the duty to disclose information which is material to patentability as defined in 37 CFR 1.56.

I hereby claim foreign priority benefits under 35 U.S.C. 119(a)-(d) or 365(b) of any foreign application(s) for patent or inventor's certificate, or 365(a) of any PCT international application which designated at least one country other than the United States of America, listed below and have also identified below, by checking the box, any foreign application for patent or inventor's certificate, or of any PCT international application having a filing date before that of the application on which priority is claimed.

Prior Foreign Application Number(s)	Country	Foreign Filing Date (MM/DD/YYYY)	Priority Not Claimed	Certified Copy Attached? YES	NO
			☐	☐	☐
			☐	☐	☐

☐ Additional foreign application numbers are listed on a supplemental priority data sheet PTO/SB/02B attached hereto.

I hereby claim the benefit under 35 U.S.C. 119(e) of any United States provisional application(s) listed below.

Application Number(s)	Filing Data (MM/DD/YYYY)

☐ Additional provisional application numbers are listed on a supplemental priority data sheet PTO/SB/02B attached hereto.

I hereby claim the benefit under 35 U.S.C. 120 of any United States application(s), or 365(c) of any PCT international application designating the United States of America, listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States or PCT International application in the manner provided by the first paragraph of 35 U.S.C. 112, I acknowledge the duty to disclose information which is material to patentability as defined in 37 CFR 1.56 which became available between the filing date of the prior application and the national or PCT international filing date of this application.

U.S. Parent Application or PCT Parent Number	Parent Filing Date (MM/DD/YYYY)	Parent Patent Number (if applicable)

☐ Additional U.S. or PCT international application numbers are listed on a supplemental priority data sheet PTO/SB/02B attached hereto.

As a named inventor, I hereby appoint the following registered practitioner(s) to prosecute this application and to transact all business in the Patent and Trademark Office connected therewith:

Name	Registration Number	Name	Registration Number
John R. Garrett	27,888	Christopher J. Reckamp	34,414
Daniel C. Crilly	38,417		
Sally Daub	41,478		

☐ Additional registered practitioner(s) named on supplemental Registered Practitioner Information sheet PTO/SB/02C attached hereto.

Direct all correspondence to:

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I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under 18 U.S.C. 1001 and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Name of Sole or First Inventor: ☐ A petition has been filed for this unsigned inventor

Given Name (first and middle [if any])	Family Name or Surname
Chak Cheung Edward	Ho

Inventor's Signature	Chak Cheung Ho	Date	OCT 4, 2000	
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Name of Additional Joint Inventor: ☐ A petition has been filed for this unsigned inventor

Given Name (first and middle [if any])	Family Name or Surname
Oleg	Drapkin

Inventor's Signature		Date	03.12.2000	
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Name of Additional Joint Inventor: ☐ A petition has been filed for this unsigned inventor

Given Name (first and middle [if any])	Family Name or Surname
Carl	Mizuyabu

Inventor's Signature		Date	Oct. 12, 2000	
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City: Thornhill	State: Ontario	ZIP: L4J 7X6	Country: Canada	

☒ Additional inventors are being named on the 1 supplemental Additional Inventor(s) sheet(s) PTO/SB/02A attached hereto.

PTO/SB/02A (3-97)

DECLARATION

ADDITIONAL INVENTOR(S)
Supplemental Sheet
Page 1 of 1

Name of Additional Joint Inventor: ☐ A petition has been filed for this unsigned inventor

Given Name (first and middle [if any])	Family Name or Surname
Ray	Chau

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Name of Additional Joint Inventor: ☐ A petition has been filed for this unsigned inventor

Given Name (first and middle [if any])	Family Name or Surname
Gordon	Caruk

Inventor's Signature	Gordon Caruk	**Date**	Oct 4/2000	
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Name of Additional Joint Inventor: ☐ A petition has been filed for this unsigned inventor

Given Name (first and middle [if any])	Family Name or Surname

Inventor's Signature		**Date**		
Residence	City:	State:	Country:	Citizenship:
Post Office Address				
City:	State:	ZIP:	Country:	

Name of Additional Joint Inventor: ☐ A petition has been filed for this unsigned inventor

Given Name (first and middle [if any])	Family Name or Surname

Inventor's Signature		**Date**		
Residence	City:	State:	Country:	Citizenship:
Post Office Address				
City:	State:	ZIP:	Country:	